

Register Map for the PCI-DAS08



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Register Description

Register overview

PCI-DAS08 registers are mapped into I/O address space. Unlike ISA bus designs, this board has *several* base addresses each corresponding to a reserved block of addresses in I/O space.

Only experienced programmers should perform direct register-level programming. We highly recommend that you use the Universal Library™ package for complete access to PCI-DAS08 functions from the full range of Windows® programming languages. The documentation for the Universal Library is available on our web site at <http://www.measurementcomputing.com/PDFmanuals/sm-ul-user-guide.pdf>.

Of the six Base Address Regions (BADR) available in the industry standard PCI 2.1 specification, two are implemented in this design and are summarized in Table 1.

Table 1. PCI-DAS08 Base Address

I/O Region	Function	Operations
BADR1	PCI Controller Operation Registers	32-bit double word
BADR2	General Control/Status Registers	16-bit word

BADR1 is likely to vary from PC-to-PC. Assigned by the PCI BIOS, these Base Address values cannot be guaranteed to be the same even on subsequent power-on cycles of the same machine. All software must interrogate BADR1 at run-time with a READ_CONFIGURATION_WORD instruction to determine the BADR_n values.

BADR1

BADR1 is reserved for the 9052 PCI Controller operations. There is no reason to access this region of I/O space for most PCI-DAS08 uses. The installation procedures and Universal Library can access all required information in this area. Unless you are writing direct register level software for the PCI-DAS08, do not concern yourself with the BADR1 address.

Interrupt status and control

BADR1 + 4Ch

This register is 32-bits long. Since the rest of the register has specific control functions, they need to be masked off in order to access the interrupt control functions.

READ/ WRITE

				11	10	9	8
				X	INTCLR	X	0
7	6	5	4	3	2	1	0
SW_INT	PCIINT	X	0	0	INT	0	INTE

Bits 1, 3, 4 and 8 must be set to 0 for proper operation of this board.

INTE is the Interrupt Enable: 0 = disabled (default), 1 = enabled.

INT is the Interrupt Status: 0 = interrupt is not active, 1 = interrupt is active.

PCIINT is the PCI Interrupt Enable: 0 = disabled (default), 1 = Enabled

SW_INT A value of 1 generates a software interrupt.

INTCLR is used to clear the Interrupt when in edge-triggered triggered configuration.

Interrupt source select

BADR1 + 50h

This register, as with all the 9052 registers, is 32-bits long. Therefore, mask off the remaining bits in order to access the OUT0 general purpose I/O bit.

31:8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	OUT0	1	0

Bit 0 Bit 0 enables the OUT0 function.
0 = enabled.
1 = disabled. Set it to "0".

Bit 1 Bit 1 selects the OUT0 bit direction.
0 = input
1 = output. Set it to "1".

OUT0 OUT0 selects the source for the interrupt:
OUT0 = 0, Interrupt input = user connector.
OUT0 = 1, Interrupt input = Counter 2 output.

BADR2

In addition to the BADR1 registers, the PCI-DAS08 uses eight consecutive addresses in the PCI I/O space (Table 2.)
Note that these registers are identical to those of the CIO-DAS08.

Table 2. BADR2 Address Map

Register	Read Function	Write Function
BADR2 + 0	A/D bits 9 - 12 (LSB)	Start eight-bit A/D Conversion
BADR2+ 1	A/D bits (MSB) 1 - 8	Start 12-bit A/D Conversion
BADR2 + 2	EOC, IP1-3, IRQ, Mux address	OP1-4, INTE, Mux address, clear interrupt
BADR2 + 3	Not Used	Not Used
BADR2 + 4	Read Counter 0 Data	Write Counter 0 Data
BADR2 + 5	Read Counter 1 Data	Write Counter 1 Data
BADR2 + 6	Read Counter 2 Data	Write Counter 2 Data
BADR2 + 7	No Readback	Control Register

A/D data registers

BADR2 + 00h

READ/WRITE

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12	0	0	0	0

LSB

READ Contains the least significant four bits of the analog input data.
WRITE Writing any data to this register causes an immediate eight-bit A/D conversion.

BADR2 + 01h

READ/WRITE

7	6	5	4	3	2	1	0
A/D1	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7	A/D8

MSB

READ Contains the most significant byte of the analog input data.

The A/D bits code corresponds to the voltage on the input according to the table below.

Decimal	Hex	Voltage Input
4095	FFF	+ 4.9976V
2048	800	0V
0	0	– 5V

WRITE Writing any data to this register causes an immediate 12-bit A/D conversion.

Status and control register

BADR2 + 02h

READ

7	6	5	4	3	2	1	0
EOC	IP3	IP2	IP1	IRQ	MUX2	MUX1	MUX0

EOC End of conversion.
 0 = A/D is not busy and data may be read.
 1 = A/D is busy.

IP3:1 Digital input bits.
IRQ Interrupt status.
 1 = positive edge detected on INT line.
 0 = cleared, by writing to BADR2 + 2h.

MUX2:0 Current Multiplexer channel, binary-coded between 0 and 7.

WRITE

7	6	5	4	3	2	1	0
OP4	OP3	OP2	OP1	INTE	MUX2	MUX1	MUX0

OP4:1 Digital output bits.
INTE Interrupt enable to the PC bus.
 1 = interrupts are enabled.
 0 = disabled.

MUX2:0 Sets current Multiplexer channel, binary-coded between 0 and 7.

Writes to this address also clear the interrupt status bit IRQ (described above).

8254 Counter 0 (User COUNTER Counter 1) Data

BADR2 + 04h

READ/WRITE

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

8254 Counter 1 (User Counter 2) Data

BADR2 + 05h

READ/WRITE

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

8254 Counter 2 (User Counter 3) Data

BADR2 + 06h

READ/WRITE

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

8254 Control Register

BADR2 + 07h

WRITE ONLY

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The control register is used to set the operating modes of 8254 counters 0,1 & 2. A counter is configured by writing the correct mode information to the control register, then writing the proper count data to the specific counter register.

The 8254 counters are 16-bit devices. Since the interface to the 8254 is only eight-bits wide, write count data to the counter register as two successive bytes; write the low byte first, then write the high byte.

For more information on the 8254 programmable interval timer, visit our web site at <http://www.measurementcomputing.com/PDFmanuals/82C54.pdf>.

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